EXPRESS MAIL NO. EL990359598US

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	: Howard C. Kirsch	Attorney Docket No.: 501214.02 (30204/US/2)
Filed	: Concurrently herewith	
Title	: SYSTEM AND METHOD TO AVOID VOLTAGE READ ERRORS IN OPEN DIGIT LINE ARRAY DYNAMIC RANDOM ACCESS MEMORIES	

INFORMATION DISCLOSURE STATEMENT

Mail Stop Patent Application
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with 37 C.F.R. §§ 1.56 and 1.97 through 1.98, applicant wishes to make known to the Patent and Trademark Office the references set forth on the attached form PTO-1449. This application relies, under 35 U.S.C. § 120, on the earlier filing date of prior Application No. 10/231,680, filed August 29, 2002. The references listed on the attached Form PTO-1449 were submitted to and/or cited by the Patent and Trademark Office in this prior application and, therefore, are not required to be provided in this application. If the Examiner wishes, copies will be provided upon request. Although the aforesaid references are made known to the Patent and Trademark Office in compliance with applicant's duty to disclose all information he is aware of which is believed relevant to the examination of the above-identified application, applicant believes that his invention is patentable.

Please acknowledge receipt of this Information Disclosure Statement and kindly make the cited references of record in the above-identified application.

Respectfully submitted,

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Form PTO-1449

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FORM PTO-1449 (REV.7-80)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. 501214.02 (30204/US/2)	APPLICATION NO. Not Yet Assigned
INFORMATION DISCLOSURE STATEMENT *(Use several sheets if necessary)*		APPLICANT(S) Howard C. Kirsch	
		FILING DATE Concurrently herewith	GROUP ART UNIT Not Yet Assigned

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	AA	5,608,668	03/04/97	Zagar	365	149	
	AB	5,844,833	12/01/98	Zagar et al.	365	149	
	AC	5,926,410	07/20/99	Raad et al.	365	63	
	AD	6,043,562	04/28/00	Keeth	257	776	
	AE	6,515,925 B2	02/04/03	Graham et al.	365	205	
	AF	6,535,439 B2	03/18/03	Cowles	365	201	
	AG	6,549,476 B2	04/15/03	Pinney	365	190	
	AH	6,566,206 B2	05/20/03	Clampitt	438	296	
	AI						
	AJ						

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO
	AK							
	AL							
	AM							
	AN							
	AO							

OTHER PRIOR ART *(Including Author, Title, Date, Pertinent Pages, Etc.)*

	AP	Sekiguchi, T. et al., "A Low-Impedance Open-Bitline Array for Multigigabit DRAM", IEEE Journal of Solid-State Circuits, Vol. 37, No. 4, April 2002, pp. 487-498.

EXAMINER	DATE CONSIDERED

* EXAMINER: Initial if reference considered, whether or not criteria is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant(s).